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EXAMINER	
RAINEY, ROBERT R	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/705,775	MAEDA ET AL.	
	Examiner	Art Unit	
	ROBERT R. RAINEY	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 December 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☒ Claim(s) *1-3, 11, 18, 19 and 21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 October 2007* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. The amendments to the claims do not render the objection to the drawings moot since the limitation cited as not being shown in the drawings was not changed at all, in for example claims 4, 7,12, and 15. As previously noted, it is examiner's belief that the drawings accurately reflect applicant's invention but that the claim language does not.

2. The amendments to the claims do not render the objection to claim 18 moot since claim 18 was not amended and the amendments of its parent claim, claim 11, don't shed light on what the difference is between calling several data lines a group or a set.

3. The amendments to claims 1-3, 19 and 21 effectively overcome the 35 USC § 112 first paragraph rejection of the claims.

4. Applicant failed to address the 35 USC § 112 first paragraph rejection of claim 18 in any way.

5. The amendments to claim 3 effectively overcome the 35 USC § 112 second paragraph rejection of claim 4 raised in the previous office action

6. Applicant's arguments with respect to the art rejections of claims 1-22, have been considered but are moot in view of the new ground(s) of rejection. However, in order to advance prosecution and for whatever applicability the arguments may have to the new rejections, examiner offers the following comments: Paragraphs 22:1 and 25:3 argue that *Sunao* does not teach shift registers used to generate timing pulses to fetch a video signal but fail to address the actual combination and arguments regarding such shift

registers in the previous office action, which combination and arguments in a somewhat more detailed form are repeated in this office action. Paragraph 22:3 seems to be an accurate description of some of the structure of applicant's disclosed invention but not all features described, for example "a sampling signal is supplied from a single circuit to every other data line", are found in the claims. Paragraph 23:1 argues limitations not found in the claims. Paragraph 23:2 seems to discuss the limitation that was deleted from the claims to overcome a new matter rejection "a sampling time of the video signal in each data signal line does not change" and seems to imply that multiphase development for high resolution is the same as that for low resolution when in fact the multiphase development changes between high and low resolution in the instant application. Paragraphs 23:3-24:3 seem to misapprehend both Sunao and applicant's disclosure. In an attempt to shed light on the issues examiner offers a detailed mapping of Sunao Fig. 1, 2, 4, and 5 to applicant's disclosed invention as shown in Fig. 6-9 with applicant's designations listed first and Sunao simplified to two adjacent lines as in applicant's drawings:

DAT1=V1, DAT2=V2, SL1=S1, SL2=S2, SL3=S5, SL4=S6, signal SMP1 = X1, signal SMP2 = X2, switches 13 = transistors 131

In Sunao as in the instant application SL1 and SL3 are always sampled at the same time, as are SL2 and SL4.

In high resolution mode both Sunao and the instant application sample SL1 and SL3 and then SL2 and SL4. Sunao Fig. 4 shows X1 active followed by

X2 active and instant application Fig. 7 shows SMP1 active followed by SMP2 active.

In low resolution mode both Sunao and the instant application sample SL1, SL2, SL3 and SL4 at the same time. Sunao Fig. 5 shows X1 and X2 active at the same time and instant application Fig. 9 shows SMP1 and SMP2 active at the same time.

Paragraphs 24:2 and 24:3 bring up multiphasing. The arguments upon which the argument about multiphasing are based are incorrect so do not support the statement that therefore Sunao cannot use multiphasing. From the above analysis it is clear that both Sunao and the instant application offer the ability to forward video signals different from each other to the video signal lines in both high and low resolution cases.

Drawings

7. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "(i) first driving in which the data signal lines of one of the data signal line groups in the block and the data signal lines of another one of the data signal line groups in the block are driven at the same time and (ii) second driving in which all the data signal lines of the data signal line groups are driven at the same time." must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Both modes as claimed require that all of the data signal lines of at least two groups of data signal lines be driven at once. Examiner believes that the claim language is in error. However, if applicant desires to keep this claim language, please identify which drawings correspond to each mode or submit new ones. Note that Figures 6 and 7, for example, cannot represent one of the modes because they show only one of the two signal lines in each group being driven at once.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

8. **Claim 18** is objected to because of the following informalities: The claim language seems to redefine terms unnecessarily. Claim 18 states that "... data signal line groups are data signal line sets ...". There is no patentably distinct difference between the terms "groups" and "sets" in the context of the claim. Appropriate correction is required.

9. **Claims 1-3, 11, 19 and 21** are objected to because of the following informalities: These claims include the new limitation "the video signal fetching section including a predetermined number of shift registers for generating a timing pulse with which the video signal is fetched from the video signal lines into the data signal lines, the shift registers being provided with respect to each block, the predetermined number of shift registers being equal to the number of data signal lines included in each data signal line group". As written "a timing pulse" fetches "the video signal" into "the data signal lines". This is true for the disclosed second driving but not the disclosed first driving. In the second driving at least two timing pulses are generated by the predetermined number of shift registers and used to fetch the video signal lines into the data signal lines. Examiner offers this as an objection based on the disclosed invention rather than a rejection for indefiniteness because the first and second driving according to the claim language could both be ones in which all of the data signal lines in the block are

sampled simultaneously. Examiner has pointed this out with regard to claims 4, 7,12, and 15 in the past and the simultaneous sampling of all of the data signal lines in the block is not precluded by the phrase "individual data signal lines of each data signal line group in the block are driven simultaneously", which was added to the independent claims to describe first driving. Appropriate correction is required.

10. **Claim 3** is objected to because of the following informalities: There are typos in the final two clauses. "t fetch" in the penultimate clause and "an all data signal lines" in the last clause.

11. **Claims 11, 19 and 21** are objected to because of the following informalities: The word "form" seems to be a typo in the final clause "to fetch the video signal form the video signal lines".

Claim Rejections - 35 USC § 112

12. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

13. Claims 18 rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in

the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 18 claims "wherein the number of divisional video signal lines is the same as the number of data signal lines connected to each of the divisional video signal lines".

Applicant does not point out support for this item and no drawing shows this. And Figure 19 contradicts this since it shows six divisional video signal lines but only four data signal lines connected to each one.

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. **Claims 1-22** are rejected under 35 U.S.C. 103(a) as being unpatentable over published Japanese Patent Application No. *JP2000-181394* ("*Sunao*") in view of applicants admitted prior art ("*APArt*") and *U.S. Patent No. 5,781,171 ("Kihara").*

Regarding **Claim 11**, *Sunao* discloses a data signal line driving circuit, which drives a plurality of data signal lines respectively so as to (i) multiphase a

video signal having a plurality of color signals and (ii) fetch the video signal into the data signal lines,

each video signal line including a plurality of divisional video signal lines divided so as to respectively correspond to the color signals (see for example VG1,VB1,VR1 etc. of Fig 12, which make up one video signal line), said circuit comprising:

data signal line groups, each including a predetermined number of adjacent data signal lines for fetching a single color signal that are sequentially connected to each divisional video signal line, the data signal line groups being regarded as a single block, the number of data signal line groups being equal to the number of video signal lines in each block; and

a video signal fetching section for fetching the video signal from the video signal lines into the data signal lines in each block,

the video signal fetching section performing

first driving in which individual data signal lines of each data signal line group in the block are driven simultaneously so as to fetch the video signal from the video signal lines into the data signal lines, and

second driving in which all data signal lines in each data signal line group in the block are driven simultaneously so as to fetch the video signal form the video signal lines into the data signal lines.

Since examiner assumes that the claim is an attempt to claim applicant's disclosed invention, assignment of data signal lines to group and block and the

first and second driving modes will be discussed by referring to applicant's disclosure. As an aid to understanding the discussion is with respect to embodiments showing video signal lines rather than divisional video signal lines. The extension from the discussed embodiment to divisional video signal lines being shown for example in Sunao Fig. 12. A detailed mapping of Sunao Fig. 1, 2, 4, and 5 to applicant's disclosed invention as shown in Fig. 6-9 with applicant's designations listed first and Sunao simplified to two adjacent lines as in applicant's drawings follows. Applicant's designations are used after the mapping to refer to both applicant's and Sunao's designations:

DAT1=V1, DAT2=V2, SL1=S1, SL2=S2, SL3=S5, SL4=S6, signal SMP1 = X1, signal SMP2 = X2, switches 13 = transistors 131.

A first data group includes SL1 and SL2, which are shown sequentially connected to DAT1. A second data group includes SL3 and SL4, which are shown sequentially connected to DAT2.

The block includes the first and second data groups.

In Sunao as in the instant application SL1 and SL3 are always sampled simultaneously, as are SL2 and SL4.

In first driving, i.e. high resolution mode, both Sunao and the instant application sample SL1 and SL3 and then SL2 and SL4. Sunao Fig. 4 shows X1 active followed by X2 active and instant application Fig. 7 shows SMP1 active followed by SMP2 active.

In second driving, i.e. low resolution mode, both Sunao and the instant application sample SL1, SL2, SL3 and SL4 at the same time. Sunao Fig. 5 shows X1 and X2 active at the same time and instant application Fig. 9 shows SMP1 and SMP2 active at the same time.

Sunao does not expressly disclose the video signal fetching section including a predetermined number of shift registers for generating a timing pulse with which the video signal is fetched from the video signal lines into the data signal lines, the shift registers being provided with respect to each block, the predetermined number of shift registers being equal to the number of data signal lines included in each data signal line group, and that in first driving all shift registers in the block are driven and in second driving one shift register in the block is driven.

Sunao, however, does further disclose the use of shift registers to generate timing signals very similar to those used for fetching the video signals and in particular first driving in which all shift registers in a block are driven to produce sequential output pulses on two output lines and second driving in which one shift register in the block is driven to produce simultaneous output pulses on the two output lines. (Referring to Fig. 4 and 9 of *Sunao* see the similarities between the timing pulses X1 and X2 that cause the video signals to be fetched from the video signal lines to the data signal lines and the signals G1 and G2 for the generation of which *Sunao* teaches the use of shift registers. The number of output lines and sequential output pulses required in a block in high resolution

mode in both cases is two. Fig. 8 teaches using two serially connected shift registers in order to generate an output pulse on the first line followed by an output pulse on the second line and also means to skip one of the shift registers and connect both output lines to the active shift register in order to produce a simultaneous output pulse on both output lines. The teaching that one shift register is required per output line provides the mapping to the number of shift registers in the block being the same as the number of video signal) Note that the switch between driving modes of the Gx signals in *Sunao* further switches between the first driving and the second driving so that the number of shift registers that operate is varied in switching between the first driving and the second driving as in claims 5, 8, 13 and 16 (see for example Fig. 8 switches 1222, 1224 and 1232) and includes stopping means for stopping operation of the shift register which is not required in driving the output signal lines after switching the drive switching circuit between the first and second driving as in claims 6, 9, 14, and 17 (See for example Fig. 8 switches 1222, 1224 and 1232 or paragraph [0014] in which is the teaching to "..stop that part and power consumption" referring to a shift register stage that is not needed because of a reduction in the number of required outputs when a lower resolution driving mode is selected.). Note also that in *Sunao* G1 and G2 are also used for fetching the video signal into data signal lines, in this case into the data signal lines of individual pixels.

Kihara discloses the use of shift registers to control sampling of signals into data signal lines (see for example items 200, 210 and 260 of Fig. 1)

APArt discloses a video signal fetching section that includes one or more shift registers for generating a timing pulse causing the video signal to be fetched from the video signal lines to the data signal lines. See for example Figure 22.

Sunao, Kihara and *APArt* are analogous art because they are from the same field of endeavor, which is video display and seek to solve the same problem, which is to reduce power consumption when switching from display of higher to lower-resolution video signals.

At the time of invention, it would have been obvious to a person of ordinary skilled in the art to modify *Sunao* according to use shift registers to generate timing signals in order to fetch data from video signal lines into data signal lines as suggested by *Kihara* and to configure the shift registers and drive switching means as taught by *Sunao* such that the video signal fetching section includes a predetermined number of shift registers for generating a timing pulse with which the video signal is fetched from the video signal lines into the data signal lines, the shift registers being provided with respect to each block, the predetermined number of shift registers being equal to the number of data signal lines included in each data signal line group, and that in first driving all shift registers in the block are driven and in second driving one shift register in the block is driven. This because one of ordinary skill at the time of the invention, familiar with the use of shift registers to generate video signal fetching signals as suggested by *Kihara* would have been able to recognize the applicability of the circuit of Sunao to the generation of the timing signals required for fetching of the

video signal into the data signal lines in *Sunao*, could have implemented the modified system and the results would have been predictable. Further suggestion/motivation would have been to provide advantages such as that given by *Sunao*, which is to lower the power consumption (see Abstract and paragraph 0014) or to use an art recognized method of generating timing signals.

Claims 4, 7, 12 and 15, are an attempt to add limitations regarding the first and second driving modes to their parent claims. The rejections of the parent claims already cover the driving modes as disclosed. As examiner has reputedly pointed out, **these claims do not seem to claim the invention**. However, for whatever value they provide, the arguments provided in the past rejection are added to those of claim 11: *Sunao*, in addition to the rejection of claim 11, discloses that the video signal fetching section includes drive switching means (claims 4 and 12) or a drive switching circuit (claims 7 and 15) for switching between (i) first driving in which the data signal lines of one of the data signal line groups in the block and the data signal lines of another one of the data signal line groups in the block are driven at the same time and (ii) second driving in which all the data signal lines of the data signal line groups are driven at the same time (Fig 1 decoder 140 and sampling signals X1, X2, X3, X4 allow any combination of the four sampling switches 131 in each data signal line group to sample the group's respective video signal clearly covering one per data signal line group and all signal lines in the signal line groups. Fig 6 illustrates all signal lines in the

groups sampling at the same time. Both modes i and ii are covered by all signal lines sampling at the same time because mode i says that one and another data signal line groups in a block, i.e. at least two data signal line groups in a block, are driven at the same time and mode ii says that all data signal line groups are driven at the same time.).

The limitations of **claims 5, 6, 8, 9, 13, 14, 16, and 17** were included in the rejection of the parent claims. The section of the parent claim rejections describing the portions of Sunao that teach the required shift register circuitry and operation is repeated here for convenience.

Note that the switch between driving modes of the Gx signals in *Sunao* further switches between the first driving and the second driving so that the number of shift registers that operate is varied in switching between the first driving and the second driving as in **claims 5, 8, 13 and 16** (see for example Fig. 8 switches 1222, 1224 and 1232) and includes stopping means for stopping operation of the shift register which is not required in driving the output signal lines after switching the drive switching circuit between the first and second driving as in **claims 6, 9, 14, and 17** (See for example Fig. 8 switches 1222, 1224 and 1232 or paragraph [0014] in which is the teaching to "..stop that part and power consumption" referring to a shift register stage that is not needed because of a reduction in the number of required outputs when a lower resolution driving mode is selected.). Note also that in *Sunao* G1 and G2 are also used for

fetching the video signal into data signal lines, in this case into the data signal lines of individual pixels.

Regarding **Claim 18**, *Sunao*, in addition to the rejection of claim 11, discloses that the data signal line groups are data signal line sets each of which is made up of a predetermined number of the data signal lines corresponding to color signals contained in the video signal fetched into the data signal lines (see for example Fig 1 and paragraph 0028 as extended to color by Fig 12 and paragraph 0101), and wherein the number of divisional video signal lines is the same as the number of data signal lines connected to each of the divisional video signal lines (examiner construes this to mean that the number of divisional video signal lines **of a given color** is the same as the number of adjacent – "adjacent" in the sense that there are no data signal lines of the given color between those connected to the divisional video signal line – data signal lines **in each block** connected to each of the divisional video signal lines; or in other words the number of divisional video signal lines of a given color is the same as the number of the video signal lines – this is the configuration already covered by the rejection of claim 11).

Claims 19 and 21 add general display system elements to the limitations or a subset of the limitations of claim 11 and are rejected on the same grounds and arguments supplemented with the following covering the system limitations:

Sunao discloses a display device, comprising: a display panel (paragraph 0105 and Figs. 13 and 14) which includes (i) a plurality of data signal lines ("S1-S4n" in Fig 1 and paragraph 0025), (ii) a plurality of scanning signal lines provided so as to cross the data signal lines (G1 to Gm in Fig 1 and paragraph 25), and (iii) pixels provided on intersections of the data signal lines and the scanning signal lines (118 in Fig 1 and paragraph 0025), a video signal for displaying an image being fetched from the data signal lines into the pixels in synchronism with a scanning signal supplied from the scanning signal lines (Figs. 1 and 4 and paragraph 0033), said video signal being retained (paragraph 0036 describes "a picture signal…written in a pixel"); and a scanning signal line driving circuit for outputting the scanning signal to the scanning signal lines in synchronism with a predetermined timing signal (Figs. 1 and 4 and paragraph 0033).

As to **claims 20 and 22**, in addition to the rejections of claims 19 and 21 respectively:

Kihara further discloses the data signal line driving circuit, the scanning signal line driving circuit, and the pixels formed on the same substrate (see Fig. 1 and paragraphs at column 6 lines 31-34 and column 11 line 62 to column 12 line 5).

At the time of invention, it would have been obvious to a person of ordinary skilled in the art to implement the above combination such that the data

signal line driving circuit, the scanning signal line driving circuit, and the pixels are formed on the same substrate as taught by *Kihara*. The suggestion/motivation would have been to reduce cost. *Kihara* does not provide motivation directly for the integrated structure but refers to it as the "so-called driver integrated structure" (see column 6, line 32) implying that this type of structure is one of well known value. Since integrating multiple devices onto a single substrate is a well know way to reduce cost, one of ordinary skill in the art at the time of the invention would have recognized its value.

Claims 1 and 2 claim methods implicit in the structure claimed in claim 11 and are rejected on the same grounds and arguments as claim 11. For reference note that claim 1 does not refer to color/divisional-video-signal-lines while claim 2 does.

Claim 3 claims a subset of the limitations of claim 11 and is rejected on the same grounds and arguments. For reference note that claim 3 does not refer to color/divisional-video-signal-lines while claim 11 does.

Claim 10 depends from claim 3 and adds limitations regarding color. Claim 10 claims a subset of the limitations of claim 18 and is rejected on the same grounds and arguments.

Comments

The comments of this "Comments" section are offered only in an attempt to further prosecution. No response is required.

By way of information: In past incarnations, claims 19 and 21 seemed to be parallel constructions in that claim 21 explicitly extended the system of claim 19 to color by the use of divisional video signal lines. The most recent amendments to the claims add color/divisional-video-signal-lines limitations to claim 19. This is not a problem. Examiner mentions it only because it seems this may have been inadvertent.

At least the clause concerning the video signal fetching section in claims 5, 8, 13, and 16 seems to have been made redundant by the limitations added to the independent claims.

Since prosecution seems stalled partly over how to describe first and second driving, examiner offers the following as a conversion into words of elements of applicant's disclosed invention according to examiner's best understanding. While some elements have never been embodied in submitted claims, this is not an indication that the language would represent a claim allowable over the prior art or even a claim free of other issues and is thus purposely not written in claim form.

n, n>1, video signal lines supply a multiphased video signal in parallel to m, m>1, data fetching blocks. nxnxm data signal lines each having an associated sampling switch that connects the data signal line to a video signal line such that nxm data signal lines are connected to each video signal line. The data signal lines divided into m sets of nxn data signal lines driving contiguous columns of a display. Each data fetching block provides means for fetching the video signal into one of the sets of data signal lines. The data signal lines within each block are divided into n groups of data signal lines, each group driving contiguous columns of the display. All data signal lines in each group of data signal lines are connected to the same video signal line. n sampling signals are provided for fetching the video signal from the video signal lines into the data signal lines in each block. n sampling switches consisting of one sampling switch in each group in the block are responsive to each sampling signal such that activation of a given sampling signal simultaneously fetches the video signal from the video signal lines into the n data lines associated with the n sampling switches. Sampling timing control circuitry comprising nxm shift registers with n shift registers provided for each block. The shift registers are connected such that the blocks are driven sequentially. The sampling timing control circuitry providing: first driving in which the n shift registers in each block are driven sequentially to provide n sequential output signals and each sampling signal in the block is responsive to a corresponding output signal such that the sampling signals in the block are activated sequentially; and second driving in which only one shift register in the block is driven to provide one output signal and all sampling signals

in the block are responsive to the one output signal such that all sampling signals in the block are activated simultaneously.

Conclusion

16. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT R. RAINEY whose telephone number is (571)270-3313. The examiner can normally be reached on Monday through Friday 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on (571) 272-7674. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/RR/

/Amare Mengistu/

Supervisory Patent Examiner, Art Unit 2629